FOCUSED ISSUE FEATURE

Future Device Modeling Trends

David E. Root

Good transistor models are essential for efficient computer-aided-design (CAD) of nonlinear microwave and RF circuits, monolithic microwave integrated circuits (MMICs), power amplifiers (PAs), and nonlinear RF systems. Increasingly complicated demands of the various semiconductor technologies (e.g., GaAs pHEMTs, InP double heterojunction bipolar transistors (DHBTs), silicon on insulator (SOI), LDMOS, GaN HFETs, etc.), and their applications in terms of power and frequency of operation and complexity of applied signals (e.g., modern communication signals with high peak-to-average ratios) have placed commensurate requirements on the accuracy and generality of the device models used for design. New semiconductor material systems (e.g., GaN) have been developing at such a fast rate that conventional compact modeling approaches may not be able to keep up. These and other challenges have spawned much research into the advanced nonlinear device modeling techniques that are the focus of this article.

The scope of this article is restricted to modeling the nonlinear device for circuit and system simulation downstream. "Device" means not only transistor but also diode or other basic nonlinear component. For clarity and consistency with common usage, the term "compact model" will be reserved for models defined by nonlinear equivalent circuits in the time domain, or, equivalently, by a system of nonlinear ordinary differential equations. Classically, compact model also meant constitutive relations [current-voltage (I-V) and charge-voltage (Q-V) relations for nonlinear lumped elements] defined by explicit closed-form expressions with parameter values specified by physics or extracted from measurements. An example is shown in Figure 1 for a generic field-effect transistor (FET) model. For this

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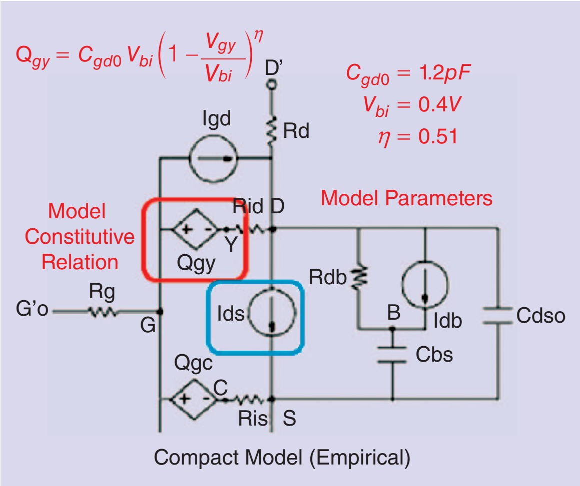

Figure 1. *A conventional compact model equivalent circuit topology for a FET. The nonlinear charge-based capacitor element is circled in red. Also shown is its constitutive relation and model parameter values.*

article, we take a somewhat more modern perspective whereby constitutive relations can include implicit expressions, tabulated relations, and numerically defined functions that can be generated by physical simulation or from measurement. In this sense, we consider the broad range of compact models, including physically based models, table-based models, and artificial neural network (ANN) models. In contrast, we use the term "behavioral model" to represent other approaches to device models. In this work, the prime example explored is that of X-parameters, a modeling (and measurement) framework defined directly in the frequency domain based on nonlinear time-invariant complex spectral maps from multitone sinusoidal input signals to output signals. The commonality here is that the device model, be it a compact model or a behavioral model, is still formulated in the language of nonlinear circuit theory. We consider a broad sample of methods and formulations, the common thread being that the circuit laws [Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL)] are being solved in the end.

Cosimulation of the actual device physical partial differential equations with compact and/or behavioral models at the circuit level is becoming more important these days. The exponential increase in computational power is making this a reality now. Multiphysics or global modeling approaches have been treated elsewhere [54], [55]. Here we simply stress that it is essential to have a good link from physical simulation to device modeling and simulation at the circuit level. This enables a seamless transition from one level of the design and technology hierarchy to the next. In this case, a device model enables the circuit consequences of various possible physical realizations of the device to be estimated prior to actual manufacturing. Later when the transistor has been made, compact or behavioral models can be extracted from measured data and the model itself refined, if necessary, as the technology matures. Technology CAD (TCAD) calculations of I-V and Q-V relationships that can be read by table-based compact models or fit as surrogates for actual measured data by extraction software (SW) are now common practices in industry as well as research labs. This useful paradigm is often known as the "virtual FAB."

Input for good compact device modeling comes not just from physics but also from measurements. Measurement data is essential, at the very least, to validate the predictions of the model so it can be used with confidence in applications. Some aspects of the device physics usually are unknown, incompletely modeled, or too complex to simulate efficiently. Empirical modeling techniques enable new semiconductor technologies to be developed into real circuits and systems long before an accurate, computationally efficient, physically based model is available in the CAD tools. It should be emphasized, however, that for an empirical model to be generally useful, the device actually characterized for model development must be representative of the population of devices from which it is selected. Great care needs to be taken to select a nominal device or an appropriate set of representative device samples prior to model parameter extraction.

This article presents a sample of advanced modeling flows constructed from a palette of characterization systems, analysis methods, and modeling formulations. The ability to mix and match basic measurement and modeling tiles enables a broad mosaic of possibilities for useful nonlinear device modeling methodologies and practical flows.

Modeling from Simple DC and Linear Data

Traditionally, measured data have been used for compact models primarily as the targets for model parameter extraction. That is, numerical values for parameters appearing in the closed-form constitutive relations of conventional empirical compact device models are chosen to provide a best fit to the measured data. The traditional approach is to extract model parameter values from simple dc and linear S-parameter measurements. The former gives information about current sources, and the later gives information about nonlinear capacitances of the model. These types of data are easy to acquire with conventional instruments.

Advanced compact models, such as the Angelov (Chalmers) model, have demonstrated very successful results for a wide variety of device technologies using primarily dc and bias-dependent S-parameter data [49]. The model constitutive relations are based on transcendental functions that are very smooth. Initial parameter extraction is based on searching for peaks in the linear transconductance characteristic versus bias, as inferred from measured S-parameter data. A good parameter extraction methodology is important to get accurate and repeatable results.

Empirical models as detailed as the Angelov model can take years of development and refinement by world-class researchers. Parameter extraction can take several days by expert modeling engineers. The extraction process is usually defined by an iterative optimization simulation loop. This process has many well-known drawbacks, including getting stuck in local minima and nonconvergence of the model for certain sets of parameter values at certain bias conditions. Often it may be impossible to achieve an accurate fit to the measured data. Usually this is because the constitutive relations, the I-V and Q-V nonlinear functions, which are prescribed by the model developer, are just too simple to fit the detailed characteristics of the transistor. Whenever a modification to a constitutive relation is made, such as to fit an unfamiliar feature of a new device, the parameter extraction flow needs to be modified as well. More details can be found in [22] and [26].

Measurement-Based Models: The Device Knows Best

From a high-level perspective, all compact models sharing the same equivalent circuit topology can be considered equivalent. That is, the dynamics (frequency dependence) of such models are determined by the types of circuit elements (current sources, nonlinear capacitors, resistors, etc.) and their arrangement in the particular equivalent circuit topology. The modeling task then reduces to identifying the functional form of the constitutive relations. If the topology, at least at the intrinsic level, is sufficiently simple, this can be accomplished by advanced fitting of the measured characteristics. Examples of this type of measurement-based approach include table-based models [23] and the more modern methods based on ANNs [24].

Measurement-based models are an outside-in approach, where parasitic elements must be identified and accounted for before the core nonlinear device model can be modeled. This is in contrast to the physically based approach, which is more of an inside-out description. In either case, nonideal parasitic effects must be accounted for. See [32] for detailed approaches to the identification and extraction of parasitic element values.

Table-Based Models

Table-based models take measured, mathematically transformed data and store the resulting discrete values of the I-V and Q-V relations in multidimensional tables. The simulator dynamically interpolates the tabulated data during simulation. There are no closed-form I-V or Q-V constitutive relations with unknown parameters in this case. In effect, the entire

From a high-level perspective, all compact models sharing the same equivalent circuit topology can be considered equivalent.

equation development and parameter extraction part of the device modeling flow is eliminated! The process of I-V measurement and numerical calculation of Q-V functions from bias-dependent S-parameter data is essentially the same for many device types (e.g., GaAs MESFETs and pHEMTs, Si MOSFETs and JFETs, etc.). This technology and process-independent measurement-based approach is therefore quite general. Physically based empirical models, in contrast, have different closed-form expressions for I-V and Q-V relations corresponding to different technologies. The measurement-based approach is also accurate because device-specific data is used to construct the nonlinear constitutive relations that define the large-signal model.

Limitations of the table-based approach come from several sources. Perhaps the most basic is the limitation of the interpolation algorithms used by the simulator to define the I-V and Q-V relations smoothly between discrete measured data points. Some table-based models have been shown to be inaccurate for simulations of high-order distortion products when the input signal magnitudes are comparable to or smaller than the distance between neighboring data points. The reason for this is that the model performance under these conditions is dominated by the details of the mathematical interpolation algorithms, rather than the underling device data [25]. Another limitation is that tables usually impose some grid-like structure on the data. Even if the data is taken on a grid of extrinsic voltages, the corresponding intrinsic voltage space is warped due to the nonlinearity of the intrinsic device [26]. This leads to the need for rereferencing equations or regridding algorithms. Other approaches, such as smoothing splines can partially mitigate these issues at the expense of additional complexity [30].

Effective hybrid methods, combining the best of empirical models with aspects of table-based models, have been proven effective in cases where the number of empirical model parameters becomes too large or where the fit to measurements requires additional accuracy. See [48] for an example that is based on the Angelov Model.

Artificial Neural Network-Based Models

The main benefits of simple measurement-based nonlinear device models can be preserved while removing most of the limitations by replacing the tables and interpolation schemes by ANNs [27], [28].

It is essential to have a good link from physical simulation to device modeling and simulation at the circuit level.

An ANN is a mathematical function, defined in terms of simple univariate nonlinear processing elements (neurons) joined together with weighted connections. For the purposes of this article, an ANN is a powerful mathematical functional approximation technique that can be used to fit any nonlinear function in any number of independent variables. The weights are determined by training algorithms effectively fitting the ANN to the measured data. ANNs are very smooth; they have nonvanishing derivatives of *infinite* order. This is a key attribute enabling accurate distortion simulations at low signal levels. ANNs are particularly convenient because they can be trained on scattered (non-gridded) data. That means, for transistor models, the intrinsic I-V and Q-V relations can be trained on the intrinsic voltage data without any regridding during processing or rereferencing during simulation. This improves both model accuracy and simulation speed.

ANNs have long played a role in microwave CAD [27], [28]. But their value for nonlinear device modeling became much more significant with the development of the so-called adjoint training method [29]. This technique enabled, for the first time, the efficient computation of smooth ANN-based constitutive relations for transistor terminal charge functions from knowledge of sampled bias-dependent capacitances such as those derived from bias-dependent S-parameter data. Adjoint training improves upon the numerical line-integration techniques of previous methods [23]. ANN-based nonlinear transistor models have demonstrated superior capabilities compared to table-based models in most respects. From the same set of data from which the above table model is constructed, the ANN model is more uniformly accurate, much smoother, and can accommodate discrete symmetry constraints such as drain-source exchange for some FET devices [38]. The combination of smooth constitutive relations that also obey exact discrete symmetry properties is especially useful for FETs used as mixers, where the instantaneous drain-source RF voltage crosses zero during operation. Finally, the ANN model can be wrapped in computational geometrical algorithms to insure robust convergence beyond the training region (region where data is

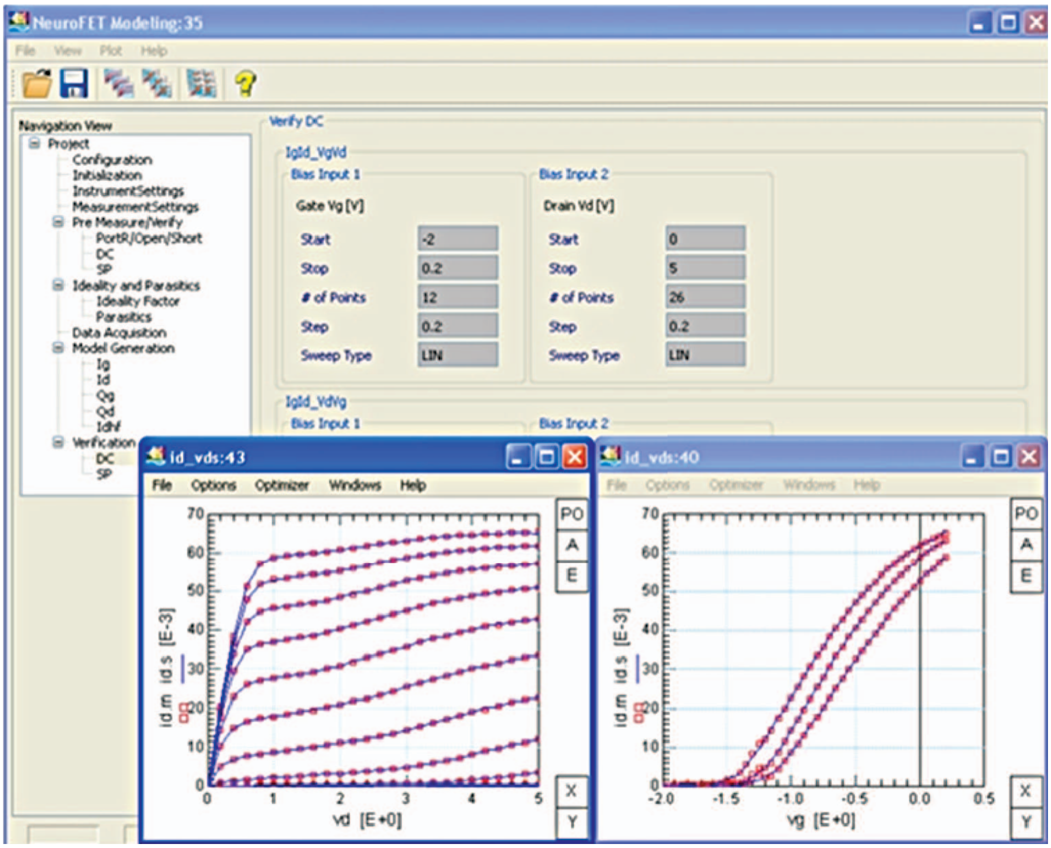

Figure 2. *The* NeuroFET *ANN-based FET model characterized and trained in Agilent IC-CAP. Measured (red symbols), simulated (blue lines).*

collected) for both improved robustness in dc, transient, and harmonic balance simulations [22]. A number of major semiconductor companies have developed and deployed such models for internal use over the last few years. Recently, a commercial ANN-based FET model with an automated data acquisition system and training SW of the type mentioned here has been released for the external market [21]. An example is given in Figure 2.

The Requirement for Richer Measurement Data

Measurement-based methods that rely on dc and linear measurements are limited, fundamentally, by the data itself. Three other modeling flows, all based on more comprehensive large-signal data, get around this limitation.

More advanced measurements, such as those made using spectrum analyzers, can provide quantitative information about distortion as a function of power. These have been proposed to be used as additional targets for optimization-based parameter extraction [20]. More recently, pulsed I-V and pulsed S-parameters have been used to extend the characterization range of devices beyond the static safe operating range and to provide what is sometimes claimed as isodynamic data [2]–[4]. This data is rich enough to help separate some of the physical effects, such as self-heating and trapping that contribute, simultaneously, to the static (dc) or small-signal response. Load-pull data in some form has been used for many years, primarily to characterize large power transistors. It has evolved from primarily scalar data used for PA performance optimization, matching network design for power, and compact model validation, to vector-based information using a VNA or sampler-based receiver. However, the information provided has usually not been sufficiently rich to enable construction of a complete transportable compact model. Recently, however, the situation has changed, dramatically, with the introduction of vector nonlinear microwave instrumentation, specifically instruments of the general class of NVNA, LSNA, and other waveform measurement systems [1], [33]–[37]. A variety of measurement systems for transistor characterization and modeling is represented in Figure 3.

NVNA Measurements for Transistors

In this section, advantages of using NVNA/LSNA measurement systems for transistor characterization for modeling are highlighted. These systems, and others with similar capabilities, are described in [1], [33]–[37], [51], [52]. In the present work, an Agilent PNA-X vector network analyzer with NVNA hardware (HW) and SW application options is used. The NVNA has two built-in microwave sources. It can control additional sources, enabling characterization of the device under test (DUT) with one or multiple large signals similar to those it may encounter in its actual applications. For large-signal periodic input stimuli, the NVNA measures the fully calibrated magnitudes and cross-frequency phases of all spectral components simultaneously incident on and scattered from each DUT port. An example is shown in Figure 4 for a two-port (three-terminal) transistor. The NVNA also controls and synchronizes dc supplies with the RF stimulus and response measurements, thereby capturing self-biasing effects needed for power-added efficiency simulations. More general measurements are possible but not considered here [1].

For the case considered here, the NVNA measures the complex-values $A_{p,k}$ and $B_{q,l}$, corresponding to the magnitudes and phases of the incident and scattered waves, respectively. The first index corresponds to the port number, and the second to the integer multiple of the fundamental frequency of the periodic stimulus. The complete time-varying voltages and currents at the device ports can be recovered from the Fourier series according to (1) and (2). The sum in (2) is over all harmonics measured within the bandwidth of the instrument. Thus the NVNA provides calibrated large-signal voltage and current waveform measurements at the input and output ports of the device, simultaneously, even under high degrees of DUT compression producing significant harmonic distortion.

$$\begin{aligned} V_{p,k}^{(peak)} &= \sqrt{2Z_0}\,.\left(A_{p,k}^{(RMS)} + B_{p,k}^{(RMS)}\right),\\ I_{p,k}^{(peak)} &= \sqrt{\frac{2}{Z_0}}\,.\left(A_{p,k}^{(RMS)} - B_{p,k}^{(RMS)}\right),\ Z_0 \in \mathbb{R}, \end{aligned} \tag{1}$$

$$\begin{aligned} V_p(t) &= \mathrm{Re}\left\{\sum_k V_{p,k}^{(peak)}\, e^{jk\omega_0 t}\right\},\\ I_p(t) &= \mathrm{Re}\left\{\sum_k I_{p,k}^{(peak)}\, e^{jk\omega_0 t}\right\}. \end{aligned} \tag{2}$$

NVNA data extends the range of device characterization well beyond that possible under dc or static operating point conditions. This is important when operating the device at large input stimulus conditions where it begins to run into limiting mechanisms of operation, such as breakdown and forward gate conduction in Schottky barrier FETs for example. The NVNA enables device data to be obtained also in regions of high-instantaneous-power dissipation. An example is given in Figure 5 for the case of a GaAs pHEMT. The measured load-line extends well beyond the range over which dc and S-parameter data can be taken. This is especially useful for high-power devices. The dynamic load-line measured by the NVNA at microwave frequencies swings into these regions for less than a nanosecond per cycle,

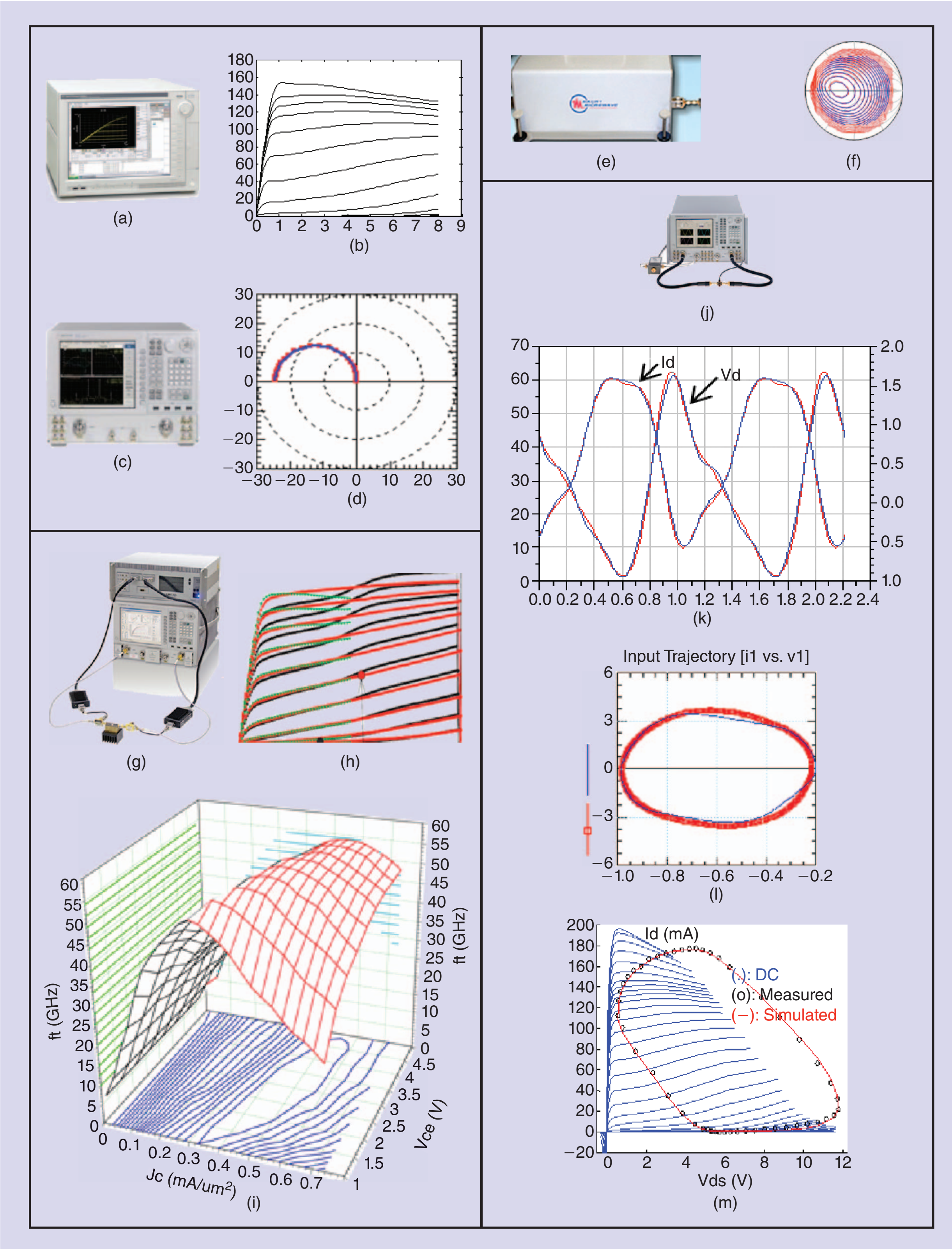

Figure 3. *A variety of measurement hardware, data, and device modeling approaches: (a) dc parameter analyzer, (b) dc I-V curves of GaAs FET, (c) linear VNA, (d) S21 versus frequency for GaAs FET, (e) passive tuner for loadpull and source-pull, (f) contours of measured (red) and simulated performance of a GaAs FET, (g) pulsed I-V and pulsed S-parameter system, (h) pulsed I-V curves from different quiescent bias points (red and black lines) and dc I-V curves (green) for a GaAs FET, (i) cutoff frequency versus current density (Jc) and Vce for a GaAs HBT computed from pulsed S-parameters, (j) NVNA system, (k) X-parameter model of GaN HEMT from NVNA data, (l) parameter extraction of GaAs FET model from NVNA data, and (m) compact model of GaAs FET from NVNA data + ANNs.*

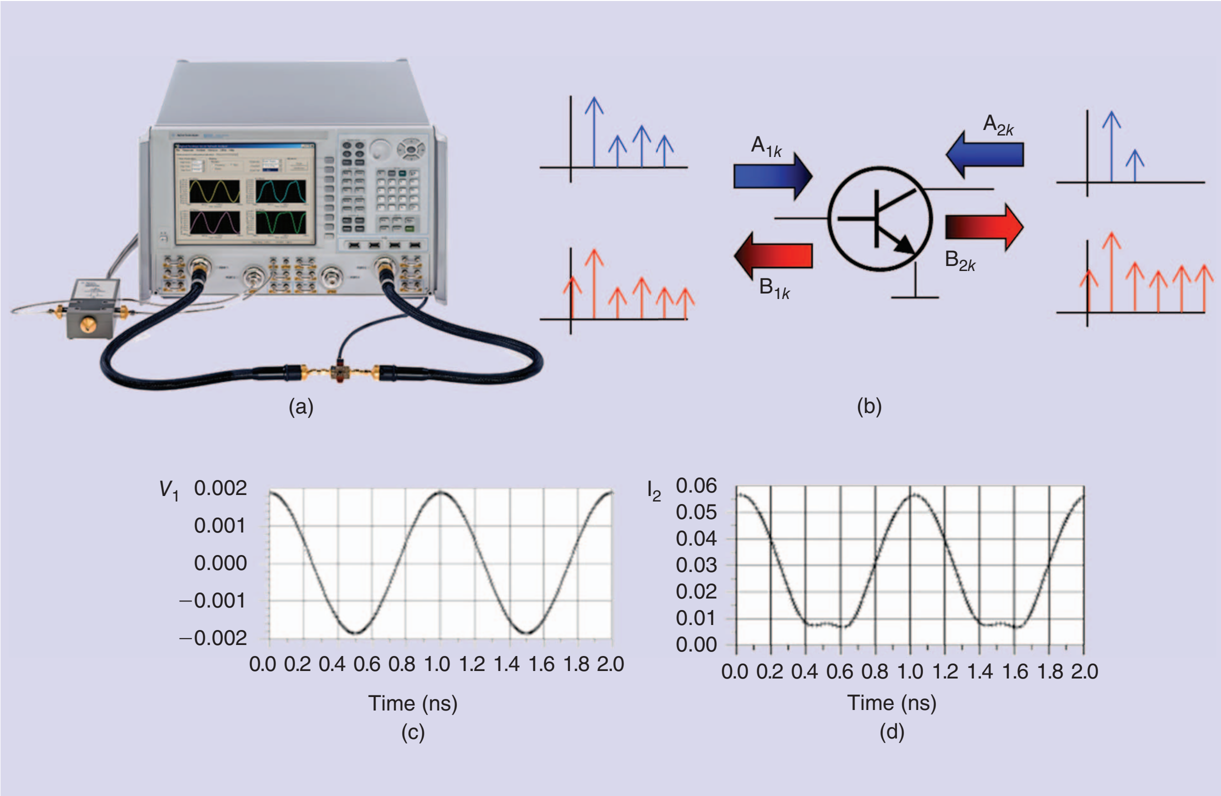

Figure 4. *(a) NVNA with phase reference, (b) DUT symbol with incident and scattered waves, (c) measured input voltage waveform, and (d) measured current output waveform in the time domain at a highly compressed operating operation.*

dramatically reducing device parametric degradation during characterization. The symbols in Figure 5 correspond to a single NVNA measurement (fixed power, complex load, frequency, and bias). By taking measurements at different values of these independent variables, a rich and comprehensive transistor characterization is obtained, covering more completely the possible DUT operating conditions than other methods.

These advantages of NVNA data persist even when compared to pulsed I-V data that have been introduced over the past years to help characterize power transistors [2]–[4]. Most practical pulsed I-V systems measure at time-scales from 100 ns to 10 μs. This is several orders of magnitude slower than the RF and microwave frequency timescales of NVNA data. Pulsed S-parameters can be taken within the bias pulses, but this gives only linearized information. Examples of pulsed I-V FET data and cutoff frequency calculations derived from pulsed S-parameter measurements of a heterojunction bipolar transistor (HBT) are shown in Figure 3.

NVNA/LSNA data is usually more representative of the large-signal behavior that the transistor will exhibit in its actual application than dc, S-parameter, and pulsed I-V and pulsed S-parameter characterization data. For example, every point on the dynamic load-line of Figure 5 corresponds to a fixed device junction temperature (isothermal condition), whereas each point on the dc I-V curves corresponds to a different junction temperature due to the different dc power dissipation. Even pulsed I-V data at timescales greater than 1 μs can be confounded by some self-heating effects, and depend sensitively on the quiescent bias point [2]. More advantages of NVNA data compared to pulsed I-V data for advanced modeling is discussed in the following.

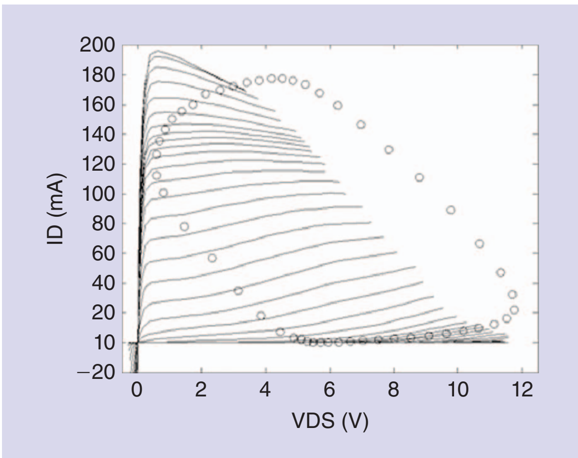

Figure 5. *An NVNA-measured dynamic load-line (O symbols), superimposed on measured dc I-V curves (lines) of a GaAs pHEMT.*

Measurement-based models are an outside-in approach, where parasitic elements must be identified and accounted for before the core nonlinear device model can be modeled.

Parameter Extraction and Validation from NVNA/LSNA Data

It is ironic that it is still common practice for nonlinear transistor models to have their parameter values extracted from dc and linear S-parameter data. A model can fit dc characteristics and S-parameters perfectly but still not give accurate results under large-signal conditions [47]. Extractions based on such simple data are therefore not reliable indicators of nonlinear model performance. For some models, generally those that include dynamic self-heating and trapping phenomena, it is impossible to properly extract the parameters from data limited to dc and S-parameters.

The most obvious modeling flow based on NVNA/LSNA data is therefore to extract and tune model parameters by directly using the NVNA large-signal measured waveforms of the device as optimization targets. That is, model parameter values are adjusted until the measured and simulated large-signal data agree [6]–[8,] [46]. As an example, a parameter extraction flow to fit NVNA waveform data is implemented in a customized Agilent IC-CAP modeling toolkit in Figure 6 for a GaAs FET.

An example of parameter extraction and model validation of the Angelov Model using LSNA data is given in [50].

Key model parameters that control limiting mechanisms of device performance, such as breakdown, and

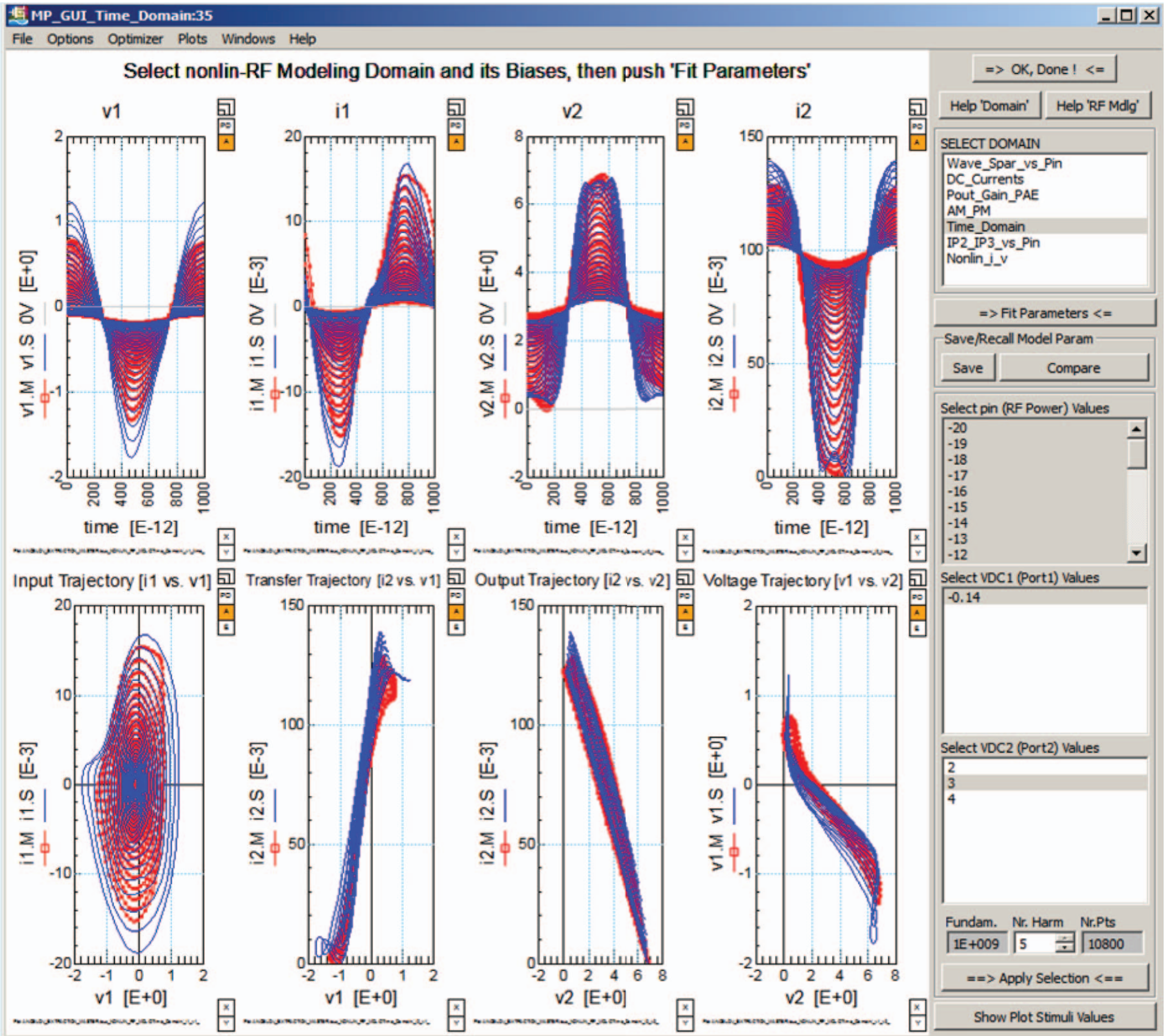

Figure 6. *A customized toolkit for Agilent IC-CAP modeling SW demonstrating parameter tuning to measured NVNA waveform data for a GaAs FET.*

Kirk effect in bipolar junction transistors (BJTs) and HBTs, for example, can be extracted more robustly and more accurately from NVNA measurements than using dc and S-parameters. Static breakdown measurements can be destructive. Breakdown behavior can depend on the time-interval over which the transistor is subjected to high fields and the device junction temperature, both of which depend on the actual large-signal waveform supported by the device. NVNA data is therefore more representative of these realistic cases. Model parameter values based on extraction to overly simple data sets, representing the device behavior under limited stimulus conditions, can cause inaccuracies when simulating device operation at high input power and high frequencies. The bottom line is that by using NVNA data, one can get the optimal parameter set for a given compact model.

On the other hand, conventional model characterization and model extraction procedures are based on choosing sets of simple measurement conditions that isolate individual contributions from different model equations to enable sensible parameter extraction. This type of approach works well in compact models that still have significant connection to some of the basic device physics, such as BJT and HBT devices. For example, forward Gummel measurements, where $V_{bc} = 0$, are routinely used to isolate and extract various diode ideality factors and saturation current parameter values, even though the transistor is usually not used under these operating conditions. Examples of this conventional approach for an advanced HBT model [43], [44] is given in [45].

A key additional benefit of the NVNA-based flow is that it inherently provides large-signal model validation for free. The waveform plots of Figure 6 show the detailed large-signal simulated model performance at high powers and microwave frequencies, compared directly to the large-signal measurements. Fundamental limitations of the model can be explored easily, and insight is provided into where the model needs to be improved [6]–[8].

Even for a model of limited capability, the ability to tune parameters enables the modeling engineer to optimize a given model for a particular application, e.g. for class C versus class A operation of the same transistor. Tradeoffs between fits to dc and S-parameters on one hand and distortion and large-signal waveforms on the other can be made quantitatively and efficiently.

Advanced Compact Models from NVNA Data

A more radical flow based on NVNA data is represented by a recently introduced method that directly constructs the large-signal constitutive relations of an advanced nonlinear electrothermal and trap-dependent time-domain model applicable to GaAs and GaN FETs [9], [31].

The equivalent circuit topology of the intrinsic model is given in Figure 7. The intrinsic model contains four coupled equivalent circuits. The top circuit models the port currents and stored device charge. The middle circuit relates electrical power dissipation to temperature. Each of the bottom two circuits models trap emission and capture processes, related to gate-lag and drain-lag phenomena, respectively [10]. Other recent work has proposed variations on the trap circuits used here. See for example [33], where cyclostationary effects are considered.

Phase control of the two-source NVNA enables active load control of the output impedance seen by the DUT. The NVNA large-signal data covers the complete range of device operation and provides validation data under realistic operating conditions. The modeling problem becomes the construction of the constitutive relations for the electrical nonlinear

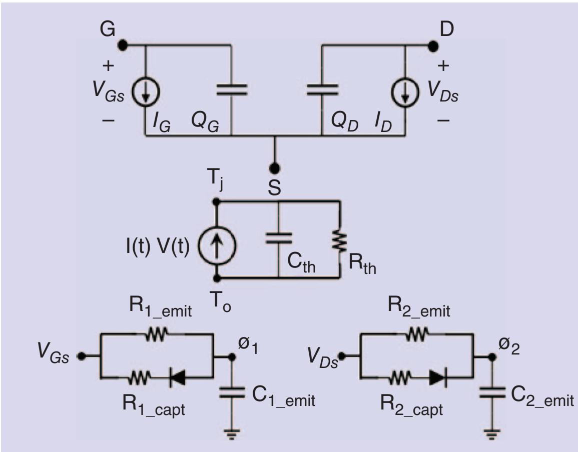

Figure 7. *Coupled equivalent circuits for an (intrinsic) electrothermal and trap-dependent III-V FET nonlinear compact model.*

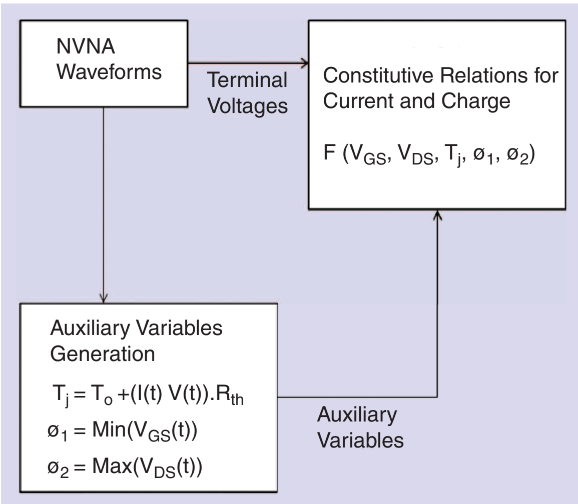

Figure 8. *NVNA waveform-based identification of current and charge nonlinear constitutive relations for the advanced FET model.*

X-parameters can very accurately model high-frequency devices that exhibit distributed effects.

elements, i.e., the functions I_G, Q_G, I_D, Q_D, as general functions not only of the intrinsic terminal voltages V_{GS}, V_{DS} but also as functions of the dynamical variables T_j, ϕ_1, and ϕ_2, representing the junction temperature and trap states associated with gate-lag and drain-lag phenomena, respectively. The NVNA waveforms, represented by over 1,000 dynamic load-lines, corresponding to different powers, loads, biases, and temperatures, are used to train ANNs to learn the complicated five-variable constitutive relations for currents and charges.

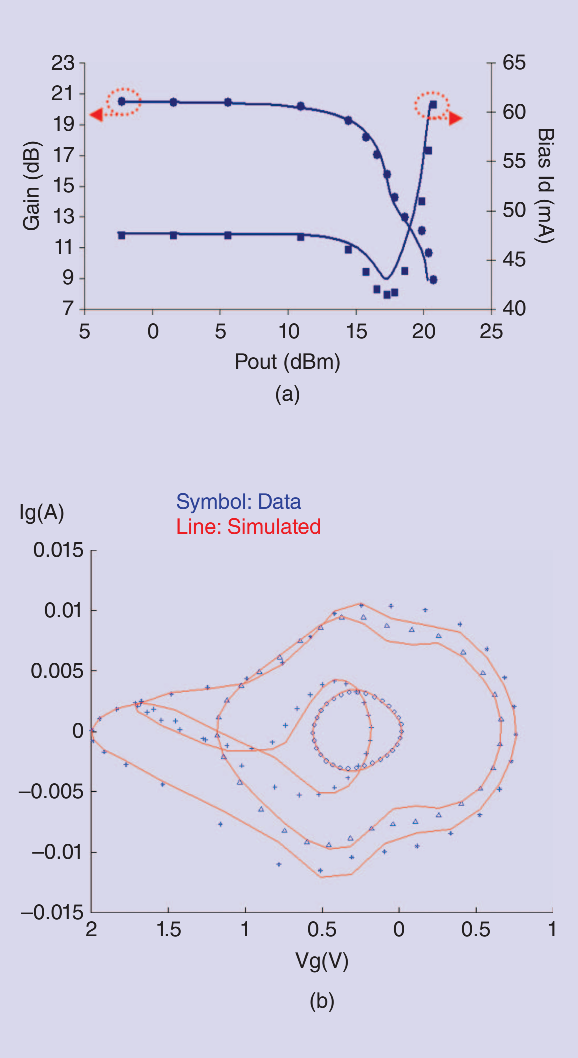

Figure 9. *A model large-signal validation of an advanced FET model for a GaAs pHEMT. (a) Gain and dc bias current versus RF output power. (b) Dynamic trajectories under complex load condition for four different power levels.*

The large-signal waveform data from the NVNA capture the steady-state response of the DUT. Assuming that the thermal time-constants and trap emission rates are much slower than the applied NVNA RF signals and that the capture rates are faster than the RF signals, the temperature and trap state voltages settle at fixed values depending on the details of the trajectories. Furthermore, these values of the dynamical variables can be calculated as simple functionals of each measured trajectory [53]. This procedure is given in Figure 8.

Many multivariate nonlinear fitting approaches could be used to define the constitutive relations at this point. But as in the case of simpler models, ANN techniques are generally preferred. The functionals expressed in Figure 8 produce values for the dependent auxiliary variables, T_j, ϕ_1, and ϕ_2, that don't fall on a grid. ANNs are easily trained on this scattered data in five dimensions. The smooth functional approximation produces excellent model behavior for the current and charge functions.

It can't be overemphasized that identifying the constitutive relations this way is both more accurate and more general than other approaches that use the same topology as Figure 7. For example, in [4] and [10], each trap state is assumed to affect the drain current only through a simple modification of the pinch-off voltage. However, there are other possible physical mechanisms, such as the virtual gate model, where the trap voltage modifies the resistance in series with the channel [11]. A great advantage of the combined NVNA and ANN training flow is that no modeling assumptions about the coupling of the trap states variables to the electrical variables are required; it is all computed automatically from the measured data.

The NVNA large-signal data is measured at gigahertz frequencies. This is fast enough to detect the trap-state dependence of the stored charges for proper nonlinear modeling of the displacement current [9]. In contrast, pulsed I-V measurements typically are made at timescales too slow to detect displacement current. Hence, there are no trap-dependence of the model charge functions in [4] and [10].

Figure 9 shows comparisons of NVNA measurements to simulations based on the above advanced compact model applied to a GaAs pHEMT device. The model predicts well the nonstandard gain compression curve and nonmonotonic bias current versus power characteristics of the measurements. This validates the model trap-dependent drain current model. The model also predicts well the measured detailed dynamic input trajectories. This validates the accuracy of the nonlinear input charge model. The transistor model almost never extrapolates during simulation because the NVNA waveform data used for characterization covered the DUT operating space so extensively.

X-Parameters for Compact and Behavioral Transistor Modeling

A quite different approach to transistor modeling with NVNA data is provided by the recent paradigm of X-parameters [12]. Whereas initially deployed for nearly matched nonlinear components and later for PAs at arbitrary load impedances and mixers, X-parameters have begun to be explored for transistor modeling applications [13]–[17]. X-parameters are the rigorous supersets of S-parameters and load-pull, applicable to both linear and nonlinear conditions. They have the same use models as S-parameters but are much more powerful. They include harmonic and intermodulation generation (frequency conversion) by the nonlinear DUT in response to large-signal stimuli.

Extracting Compact Model Parameters by Optimizing to Measured X-Parameters

The measurement and extraction process of X-parameters separates out the effects of unwanted source harmonics and instrument multifrequency mismatch. X-parameters therefore represent intrinsic DUT nonlinear properties properly referenced to an ideal stimulus condition and ideal loads. These features make measured X-parameters especially good target data for parameter extraction of empirical nonlinear models. Extracting compact model parameters to measured X-parameters has all the benefits of extracting to waveform NVNA data, as discussed previously, with the additional advantage of the X-parameter data being less biased by system impairments. This extraction method therefore yields more consistent results across different nonlinear instruments.

X-Parameter-Based Transistor Models in the Frequency Domain

S-parameters are not only familiar and reliable small-signal measurements but they also provide a complete behavioral description of a linear time-invariant component. Analogously, X-parameters are fully calibrated large-signal measurements that also provide a native frequency domain behavioral representation of a nonlinear component. X-parameters are rigorous supersets of S-parameters that reduce exactly to S-parameters in the small signal limit. They constitute a black-box approach that can be directly measured on transistors manufactured in any technology, provided the power requirements can be handled by an appropriate test set and the frequencies are within the bandwidth of the instrument. X-parameter behavioral models for transistors are especially useful for new device technologies where there may not be a suitable compact model available or where the compact model intellectual property (IP) needs to be protected. X-parameters provide a model at the external terminals of the device. This means there is no need to define an internal model structure such

Limitations of the table-based approach come from several sources.

as an equivalent circuit topology. Because the approach is native to the frequency domain, X-parameters can very accurately model high-frequency devices that exhibit distributed effects. A limitation, however, is that X-parameters are not available for simulation in conventional transient analysis.

X-parameters start from the set of incident and scattered complex phasors of Figure 4(b) and define from them nonlinear time-invariant spectral maps that, in principle, completely specify the steady-state large-signal component behavior [12], [40]. For transistors, a convenient and practical approximation to the general X-parameter equations takes the form of (3). The corresponding equations for the port dc-currents, not shown, are needed to complete the DUT description

$$\begin{aligned} B_{p,k} &= X^{(F)}_{p,k}(LSOP)P^{k} \\ &\quad + \sum X^{(S)}_{p,k;p',k'}(LSOP)P^{k-k'}A_{p',k'} \\ &\quad + \sum X^{(T)}_{p,k;p',k'}(LSOP)P^{k+k'}A^{*}_{p',k'}, \\ LSOP &= (V_1, V_2, |A_{1,1}|, A_{2,1}P^{-1}). \end{aligned} \tag{3}$$

There are three types of X-parameter functions in (3), specified by the superscripts F, S, and T, respectively. Each X-parameter function is evaluated at the periodic time-varying large-signal operating point $LSOP$, established by the DUT in response to the specific applied dc bias voltages V_1 and V_2 and the two large-signal sinusoidal signals at the fundamental frequency $A_{1,1}$ and $A_{2,1}$, simultaneously incident at the two DUT ports [12]. Here, $P = e^{j\phi(A_{1,1})}$ contains the phase of $A_{1,1}$ and simplifies the notation. The sinusoidal input signals define a harmonic frequency grid for the response frequency components, indexed by integer k (and k').

The $X^{(F)}_{p,k}$ functions in (3) model the DUT responses at each port p and harmonic k to the ideal two-tone large-amplitude stimuli, assuming perfect matching at each harmonic frequency at each port.

The $X^{(S)}_{p,k;p',k'}$ and $X^{(T)}_{p,k;p',k'}$ terms model the DUT's first-order sensitivities to mismatch at harmonic frequencies. Mismatch at one harmonic frequency can affect the DUT response at other harmonic frequencies and even dc. Note these sensitivities themselves depend in a nonlinear way on the $LSOP$. The model accurately predicts the effects of mismatch as long as the incident harmonic signals and the DUT dependence on these additional harmonic signals are not both large. This is the harmonic superposition principle [42], which is an approximation used for practical convenience. It too can be relaxed, if necessary, by using more independent spectral frequencies in the nonlinear mapping (less spectral linearization).

We will see how effective this approximation is below even for DUTs where harmonic terminations are important to the device operation. More details are given in [12], [15], and [41].

Identifying the X-parameter model based on the approximation of (3) requires controlling a range of dc biases on the two ports, independently varying the input power, and also varying both the incident wave amplitude and relative phase of the injected signal at the output port.

The $X^{(S)}_{p,k;p',k'}$ terms are somewhat analogous to so-called power-dependent S-parameters (sometimes called "hot S-parameters"), because their values depend on power (and load), while their contributions to the DUT responses are proportional to the small-signal phasors $A_{p',k'}$. But the $X^{(S)}_{p,k;p',k'}$ terms include, in addition, the transfer functions from stimuli at one frequency to responses at another. The final terms, $X^{(T)}_{p,k;p',k'}$, also contribute to multifrequency mismatch sensitivity and account for independent contributions to the scattered waves from the conjugate phasors, $A^{*}_{p',k'}$, for which there is no analogue in linear S-parameter theory. These contributions can be related to the image spectral responses from the self-mixing processes of the DUT, driven by time-varying large signals, as it scatters additional small signals that map onto the harmonic output spectrum. Both the $X^{(S)}_{p,k;p',k'}$ and $X^{(T)}_{p,k;p',k'}$ terms, taken together, are required to predict the sensitivities to harmonic mismatch effects of the nonlinear component when driven by one or more large-signal sinusoidal signals. Failure to account for the $X^{(T)}_{p,k;p',k'}$ contributions is the reason that hot S-parameters and also large-signal S-parameters are fundamentally incomplete, nonpredictive, and ultimately flawed methodologies.

While (3) may look complicated, the X-parameter functions are automatically measured by the NVNA at the user-specified set of bias conditions, RF signal power levels, and relative phase of the two

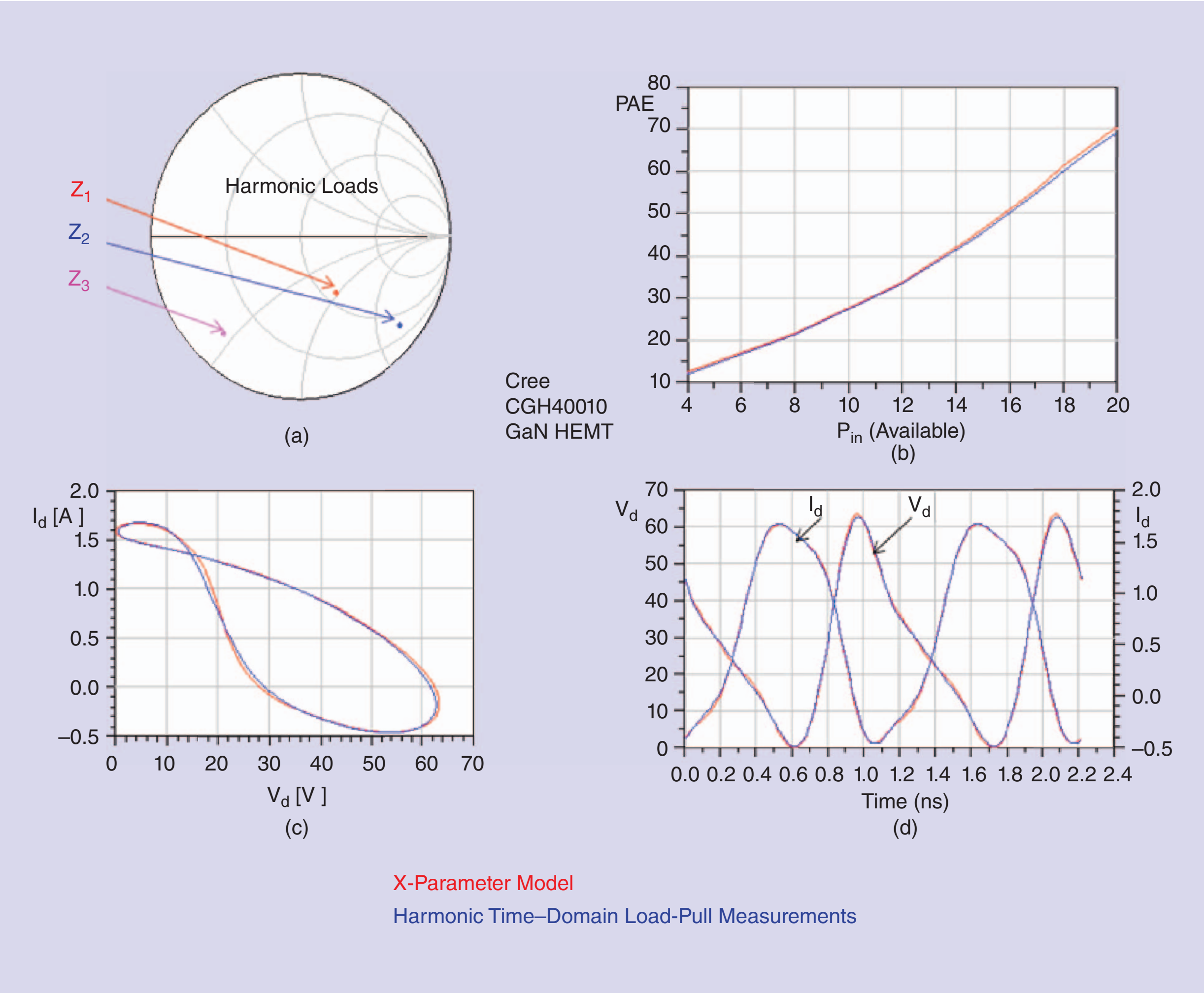

Figure 10. *A load-dependent X-parameter model validation for a GaN HEMT. X-parameter model simulations (red) and measured time-domain harmonic load-pull validation measurements (blue). (a) Fundamental and harmonic loads, (b) power added efficiency versus input power, (c) dynamic loadline, and (d) I_d and V_d waveforms.*

large signals that must be swept for a complete DUT description. To extract the harmonic sensitivity functions in (3), an additional (third) source is added and controlled by the NVNA. The sampled X-parameter function values at the measurement points are saved to a multidimensional file that is read and interpolated dynamically during simulation.

A load-dependent X-parameter model using (3) was developed for a 10-W GaN packaged transistor in [15]. The model was validated with much more extensive time-domain harmonic load-pull measurements. Results are summarized in Figure 10 for a particular set of harmonic impedances and a wide range of input power. The harmonic sensitivity terms of (3) for this X-parameter model were measured at controlled fundamental load conditions, using a single load tuner at the fundamental frequency. (Active source injection at the output port at the fundamental frequency is an alternative method.) Harmonic impedances were uncontrolled; the tuner provides various values of harmonic impedances as it moves from one fundamental complex load state to the next. Nevertheless, the resulting X-parameter model was demonstrated to predict accurately the DUT response to independently tuned (controlled) harmonic impedances over the entire Smith chart. The time-domain harmonic load-pull characterization required three independent load tuners, one each for the fundamental, second, and third harmonics, respectively, at the output. This demonstration is a direct experimental validation of the harmonic superposition principle that led to (3). This predictive capability of X-parameters dramatically reduces the HW complexity, number of measurements, and resulting data file size for the design of high-efficiency amplifiers where harmonic terminations may

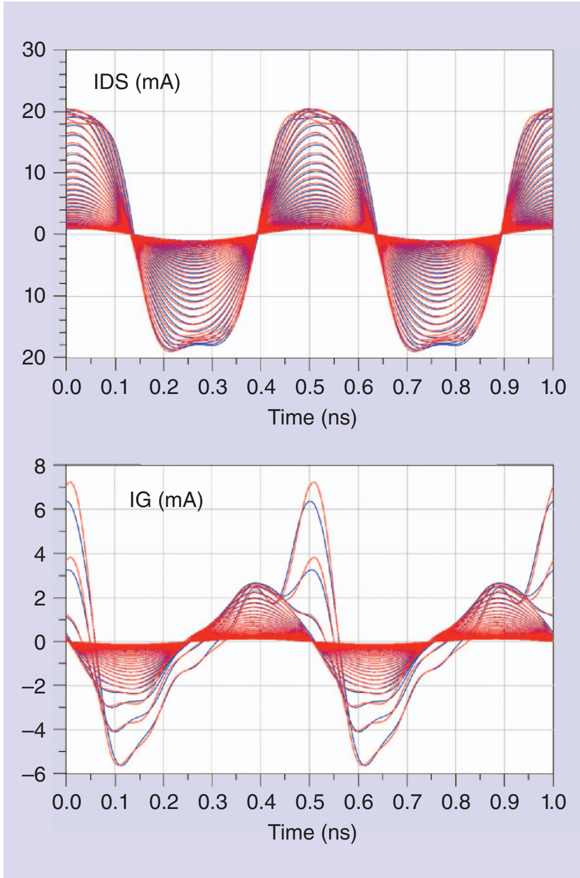

Figure 11. *Waveforms from measured X-parameters of a 4x30 µm pHEMT device (red) compared to waveforms from X-parameters measured on a 4x60-µm device but mathematically scaled to 4x30 µm (blue).*

still have significant influence on the DUT behavior. Additional benefits and comparisons are presented

TABLE 1. Simplified comparison of conventional compact models and X-parameter device models.

Approach	Advantages	Disadvantages
Conventional compact transistor models	• Work in all simulation modes (TA, HB, CE) • Simple statistics through PDF of parameters • Noise models common • Dynamic self-heating common (memory) • What-if scenarios possible	• Development time long; expert required • Extraction difficult; time-consuming • Technology-specific • Key physics may not be included
X-parameter transistor model	• Technology independent • Very accurate within characterization range • Complete IP protection • Works for packaged parts • Automated extraction • Convergence often better than compact models	• Limited by NVNA BW • Works only in frequency or envelope domain, not TA • Large file size for comprehensive model
	Memory effects demonstrated Scalability demonstrated	

in [15]. Should the refection coefficient at a harmonic and the DUT dependence to harmonic injection both be very large, the X-parameter framework can treat the harmonic incident waves without the linearity assumption by suitable modification of (3).

Recently, the capability to scale X-parameters from actual measurements on a given device layout to predict the X-parameters of transistors of scaled layouts was demonstrated [16], [17]. An example of such a result is given in Figure 11 [17]. X-parameter-based transistor models can therefore be endowed with geometrical scaling capabilities consistent with functionality expected from traditional compact time-domain models. This enhancement could extend the applicability of X-parameter measurements and modeling to MMIC design by providing, for example, the IC designer with a continuously variable FET total gate width design degree of freedom from measured X-parameters on a particular test structure.

Other early limitations of commercial X-parameter implementations, such as the lack of dynamic memory effects, have been addressed in research over the last few years with very promising results [18], [19]. It may not be very long before these and other advanced enhancements are more widely deployed.

A rough comparison between conventional compact transistor models in the time domain and X-parameter-based transistor models is given in Table 1.

Conclusion

Several advanced compact and behavioral transistor modeling techniques have been presented and contrasted. Distinct measurement approaches can be combined with the different modeling approaches to create many powerful end-to-end methodologies to suit a variety of needs. The recent commercial availability of NVNA/LSNA instruments enables many new and powerful transistor modeling flows. Several such methodologies were examined in this review. Parameter extraction, model tuning, and large-signal validation of conventional empirical compact models using NVNA waveform and X-parameter data was shown to have substantial advantages compared to approaches based on more traditional data sets. NVNA waveform data combined with advanced ANN modeling technology produced a large-signal electrothermal and trap-dependent nonlinear time-domain model for III-V FET devices with advanced memory effects, high accuracy, and considerable generality. This flow actually bypasses the need for explicit model constitutive relation formulation by automatically providing comprehensive coupling of electrical and other dynamical variables with a minimum of assumptions. Finally, advances in X-parameter measurement and behavioral modeling techniques show promise for applications at the individual transistor level. These are trends that are becoming useful now and are likely to become increasingly important in the future.

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References

[1] *PNA-X Nonlinear Vector Network Analyzer (NVNA) (Options 510, 514, 518, and 520).* (2012) [Online]. Available: http://www.agilent.com/find/nvna

[2] A. E. Parker and D. E. Root, "Pulse measurements quantify dispersion in PHEMTs," in *Proc. URSI Int. Symp. Signals, Systems, Electronics,* Sep. 1998, no. 98, pp. 444–449.

[3] J. P. Teyssier, P. Bouysse, Z. Ouarch, D. Barataud, T. Peyretaillade, and R. Quere, "40 GHz/150 ns versatile pulsed measurement system for microwave transistor isothermal characterization," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 12, pp. 2043–2052, Dec. 1998.

[4] T. Gasseling, "Compact transistor models: The roadmap to first pass amplifier design success," *Microw. J.*, Mar. 2012.

[5] *Advanced Design System Documentation: Nonlinear Devices*, Agilent Technologies, Santa Clara, CA.

[6] E. Vandamme, W. Grabinski, D. Schreurs, and T. Gneiting, "Large-signal network analyzer measurements and their use in device modeling," i*n Proc. MIXDES 2002*, Wroclaw, Poland, pp. 1–24.

[7] F. Sischka, "Improved compact models based on NVNA measurements," in *Proc. European Microwave Week 2010 Workshop*, Paris, France.

[8] F. Sischka, "Nonlinear network analyzer measurements for better transistor modeling," in *Proc. IEEE Conf. Microelectronic Test Structures, Amsterdam,* The Netherlands, Apr. 2011, pp. 95–100.

[9] J. Xu, J. Horn, M. Iwamoto, and D. E. Root, "Large-signal FET model with multiple time scale dynamics from nonlinear vector network analyzer data," in *IEEE MTT-S Int. Microwave Symp. Dig.*, May 2010, pp. 1–4.

[10] O. Jardel, F. De Groote, T. Reveyrand, J.-C. Jacquet, C. Charbonniaud, J.-P. Teyssier, D. Floriot, and R. Quere, "An electrothermal model for AlGaN/GaN power HEMTs including trapping effects to improve large-signal simulation results on high VSWR," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 12, pp. 2260–2269, Dec. 2007.

[11] A. M. Conway and P. M. Asbeck, "Virtual gate large signal model of GaN HFETs," in *Proc. IEEE MTT-S Int. Microwave Symp.*, 2007, pp. 605–608.

[12] D. E. Root, "X-parameters: The emerging paradigm for interoperable characterization, modeling, and design of nonlinear microwave and RF components and systems," in *Proc. IEEE Wamicon Tutorial*, Clearwater, FL, Apr. 2011, pp. 1–62.

[13] C.-S. Chiu, K.-M. Chen, G.-W. Huang, C.-H. Hsiao, K.-H. Liao, W.-L. Chen, S.-C. Wang, M.-Y. Chen, Y.-C. Yang, K.-L. Wang, L.-K. Wu, "Characterization of annular-structure RF LDMOS transistors using polyharmonic distortion model," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2009, pp. 977–980.

[14] G. Simpson, J. Horn, D. Gunyan, and D. E. Root, "Load-pull + NVNA = Enhanced X-parameters for PA designs with high mismatch and technology-independent large-signal device models," in *Proc. IEEE ARFTG Conf.*, Portland, OR, Dec. 2008, pp. 88–91.

[15] J. Horn, D. E. Root, and G. Simpson, "GaN device modeling with X-parameters," in *Proc. IEEE Compound Semiconductor Integrated Circuits Symp.*, 2010, pp. 1–4.

[16] J. G. Leckey, "A scalable X-parameter model for GaAs and GaN FETs," in *Proc. European Microwave Integrated Circuits Conf.*, 2011, pp. 13–16.

[17] D. E. Root, M. Marcu, J. Horn, J. Xu, R. M. Biernacki, and M. Iwamoto, "Scaling of X-parameters for device modeling," in *Proc. IEEE Int. Microwave Symp.*, Jun. 2012, pp. 1–3.

[18] J. Verspecht, J. Horn, L. Betts, D. Gunyan, R. Pollard, C. Gillease, and D. E. Root, "Extension of X-parameters to include long-term dynamic memory effects," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2009, pp. 741–744.

[19] A. Soury and E. Ngoya, "Handling long-term memory effects in X-parameter model," in *Proc. IEEE Int. Microwave Symp.*, Jun. 2012, pp. 1–3.

[20] J. W. Bandler, Q.-J. Zhang, S. Ye, and S. H. Chen, "Efficient large-signal FET parameter extraction using harmonics," *IEEE Trans. Microw. Theory Tech.*, vol. 37, no. 12, pp. 2099–2108, 1989.

[21] *W8531EP IC-CAP NeuroFET Extraction Package.* (2012) [Online]. Available: http://www.agilent.com/find/eesof-neurofet

[22] D. E. Root, J. Xu, M. Iwamoto, and D. Gunyan, "Nonlinear FET modeling fundamentals and neural network applications," in *Proc. IEEE Int. Microwave Symp. Workshop*, 2007.

[23] D. E. Root, S. Fan, and J. Meyer, "Technology independent non quasi-static FET models by direct construction from automatically characterized device data," in *Proc. 21st European Microwave Conf.*, Stuttgart, Germany, Sep. 1991 pp. 927–932.

[24] J. Xu, D. Gunyan, M. Iwamoto, A. Cognata, and D. E. Root, "Measurement-based non-quasi-static large-signal FET model using artificial neural networks," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Jun. 2006 pp. 469–472.

[25] D. J. McGinty, D. E. Root, and J. Perdomo, "A production FET modeling and library generation system," in *IEEE GaAs MANTECH Conf. Tech. Dig.*, San Francisco, CA, Jul. 1997, pp. 145–148.

[26] D. E. Root, J. Xu, J. Horn, and M. Iwamoto, "The large-signal model: Theoretical foundations, practical considerations, and recent trends," in *Nonlinear Transistor Model Parameter Extraction Technique*. Cambridge, U.K.: Cambridge Univ. Press, Oct. 2011, ch. 5.

[27] Q. J. Zhang and K. C. Gupta, *Neural Networks for RF and Microwave Design*. Norwood, MA: Artech House, 2000.

[28] S. Haykin, *Neural Networks: A Comprehensive Foundation*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1999.

[29] J. Xu, M. C. E. Yagoub, R. Ding, and Q. J. Zhang, "Exact adjoint sensitivity analysis for neural based microwave modeling and design," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 1, pp. 226–237, 2003.

[30] V. Cuoco, M. P. van den Heijden, and L. C. N. de Vreede, "The "Smoothie" data base model for the correct modeling of non-linear distortion in FET devices," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2002, pp. 2149–2152.

[31] P. Roblin, D. E. Root, J. Verspecht, Y. Ko, and J. P. Teyssier, "New trends for the nonlinear measurement and modeling of high-power RF transistors and amplifiers with memory effects," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1964–1978, 2012.

[32] M. Rudolph, C. Fager, and D. E. Root, Eds., *Nonlinear Transistor Model Parameter Extraction Techniques.* Cambridge, U.K.: Cambridge Univ. Press, 2011.

[33] P. Roblin, *Nonlinear RF Circuits and Nonlinear Vector Network Analyzers.* Cambridge, U.K.: Cambridge Univ. Press, 2011, ch. 2.

[34] T. Williams, O. Mojon, S. Woodington, L. Simon, J. Lees, M. Barciela, F. J. Benedikt, and P. J. Tasker, "A robust approach for comparison and validation of large signal measurement systems," in *Proc. IEEE MTT-S Int. Microwave Symp.*, Jun. 2008, pp. 257–260.

[35] D. Barataud, M. Campovecchio, and J.-M. Nebus, "Optimum design of very high-efficiency microwave power amplifiers based on time-domain harmonic load-pull measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 49, no. 6, pp. 1107–1112, Jun. 2001.

[36] P. Blockley, D. Gunyan, and J. B. Scott, "Mixer-based, vector-corrected, vector signal/network analyzer offering 300 kHz–20 GHz bandwidth and traceable phase response," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2005, pp. 1497–1500.

[37] J. Verspecht, P. Debie, A. Barel, and L. Martens, "Accurate on wafer measurements of phase and amplitude of the spectral components of incident and scattered voltage waves at the signal port of a nonlinear microwave device," in *Proc. IEEE MTT-S Int. Microwave Symp.*, 1995, pp.1029–1032.

[38] J. Xu, D. Gunyan, M. Iwamoto, J. Horn, A. Cognata, and D. E. Root, "Drain-source symmetric artificial neural network-based FET model with robust extrapolation beyond training data," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Honolulu, HI, Jun. 2007, pp. 2011–2014.

[39] P. J. Tasker, M. Demmler, M. Schlechtweg, and M. Fernandez-Barciela, "Novel approach to the extraction of transistor parameters from large signal measurements," in *Proc. 24th European Microwave Conf.*, Sep. 1994, pp. 1301–1306.

[40] J. Verspecht and D. E. Root, "Poly-harmonic distortion modeling," *IEEE Microw. Mag.*, vol. 7, no. 3, pp. 44–57, Jun. 2006.

[41] D. E. Root, J. Verspecht, D. Sharrit, J. Wood, and A. Cognata, "Broad-band, poly-harmonic distortion (PHD) behavioral models from fast automated simulations and large-signal vectorial network measurements," *IEEE Trans. Microw. Theory Tech.*, vol. 53. no. 11, pp. 3656–3664, Nov. 2005.

[42] J. Verspecht, M. vanden Bossche, and F. Verbeyst, "Characterizing components under large signal excitation: Defining sensible "large signal S-parameters"?!" in *49th IEEE ARFTG Conf. Dig.*, 1997. pp. 109–117.

[43] M. Iwamoto, D. E. Root, J. B. Scott, A. Cognata, P. M. Asbeck, B. Hughes, and D. C. D'Avanzo, "Large-signal HBT model with improved collector transit time formulation for GaAs and InP technologies," in *IEEE MTT-S Int. Microwave Symp. Dig.*, Philadelphia, PA, Jun. 2003, pp. 635–638.

[44] M. Iwamoto and D. E. Root, "Large-signal III–V HBT model with improved collector transit time formulations, dynamic self-heating, and thermal coupling," in *Proc. IEEE Int. Workshop Nonlinear Microwave Millimeter Wave Integrated Circuits*, Rome, Italy, Nov. 2004.

[45] M. Iwamoto, J. Xu, and D. E. Root, "DC and thermal modeling: III–V FETs and HBTs," in *Nonlinear Transistor Model Parameter Extraction Techniques.* Cambridge, U.K.: Cambridge Univ. Press, 2011, ch. 2.

[46] W. Grabinski, E. P. Vandamme, D. Schreurs, H. Maeder, O. Pilloud, and C. C. McAndrew, "5.5 GHz LSNA MOSFET modeling for RF CMOS circuit design," in *60th IEEE ARFTG Conf. Dig.*, 2002, pp. 39–47.

[47] M. Pirola, D. E. Root, and G. Ghione, "Large-signal performance of measurement-based diode models for nonlinear circuit simulation: A comparison," in *Proc. 25th European Microwave Conf.*, 1995, pp. 1006–1010.

[48] I. Angelov, N. Rorsman, J. Stenarson, M. Garcia, and H. Zirath, "An empirical table-based FET model," *IEEE Trans. Microw. Theory Tech.*, vol. 47, pp. 2350–2357, Dec. 1999.

[49] I. Angelov, L. Bengtsson, and M. Garcia, "Extensions of the chalmers nonlinear HEMT and MESFET model," *IEEE Trans. Microw. Theory Tech.*, vol. 46, no. 10, pp. 1664–1674, Oct. 1996.

[50] I. Angelov, M. Thorsell, K. Andersson, N. Rorsman, and H. Zirath, "Recent results on using LSVNA for compact modeling of GaN FET devices," in *Proc. IEEE Int. Microwave Symp. Workshop: Device Model Extraction Large-Signal Measurements*, Montreal, QC, Canada, Jun. 2012.

[51] W. Van Moer and Y. Rolain, "A large-signal network analyzer: Why is it needed?" *IEEE MTT-S Microw. Mag.*, vol. 7, no. 6, pp. 46–62, 2006.

[52] W. Van Moer and L. Gomme, "NVNA versus LSNA: Enemies or friends?" *IEEE MTT-S Microw. Mag.*, vol. 11, no. 1, pp. 97–103, 2010.

[53] D. E. Root, J. Xu, J. Horn, and M. Iwamoto, "The Large-Signal Model: theoretical foundations, practical considerations, and recent trends," in *Nonlinear Transistor Model Parameter Extraction Techniques*. Cambridge, U.K.: Cambridge Univ. Press, Oct. 2011, Ch. 5

[54] P. H. Aaen; J. Wood, D. Bridges, L. Zhang, E. Johnson, T. Barbieri, J. Pla, C. M. Snowden, J. P. Everett, J. M. Kearney, "Multi-physics modeling of high-power microwave transistors," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2012, pp. 1–3.

[55] M. B. Steer, "Multiphysics multiscale modeling of microwave circuits and systems hybridizing circuit, electromagnetic and thermal modeling," *15th International Conference on Microwaves, Radar and Wireless Communications*, 2004, vol. 3, pp. 1097–1105.

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